Electronic Version
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Claims

[c1] 1. A flip-chip substrate, wherein at least a chip is attached to the flip-chip substrate and the chip has an active surface with a plurality of bonding pads and each bonding pad has a bump thereon, the substrate comprising:
a plurality of contact pads embedded in the substrate, wherein locations of the contact pads are arranged corresponding to locations of the bonding pads on the chip, wherein any two contact pads align with their two corresponding bonding pads at a melting point of the bumps.

[c2] 2. The flip-chip substrate of claim 1, wherein the substrate has a coefficient of thermal expansion greater than that of the chip.

[c3] 3. The flip-chip substrate of claim 2, wherein a distance between any two bonding pads is greater than a distance between their two corresponding contact pads at room temperature.

[c4] 4. The flip-chip substrate of claim 1, wherein the contact pads are arranged in arrays.

[c5] 5. The flip-chip substrate of claim 1, wherein the bonding pads and the bumps are arranged in arrays.

[c6] 6. The flip-chip substrate of claim 1, wherein one of the contact pads serves as a first expansion reference mark and one of the bonding pads corresponding to the first expansion reference mark serves as a second expansion reference mark such that the first expansion reference mark on the substrate is aligned to the second expansion reference mark on the chip.

[c7] 7. The flip-chip substrate of claim 6, wherein the first expansion reference mark is located at a center of a distribution region of the contact pads.

[c8] 8. The flip-chip substrate of claim 6, wherein the second expansion reference mark is located at a center of a distribution region of the bonding pads.

[c9] 9. The flip-chip substrate of claim 1, wherein the substrate has a plurality of cavities and each contact pad is exposed by one cavity.

[c10] 10. A flip-chip bonding process for attaching a chip and a substrate, wherein the chip has an active surface with a plurality of bonding pads thereon, and each bonding pad has a bump thereon, wherein one of the bumps serves as a first expansion reference mark, the substrate has a

plurality of cavities corresponding to the bumps and each cavity exposes one contact pad, wherein one of the cavities serves as a second expansion reference mark, the flip-chip bonding process comprising the steps of: aligning the first expansion reference mark on the chip with the second expansion reference mark on the substrate and placing the chip onto the substrate; and conducting a reflow process so that the bumps and their corresponding cavities bond together, wherein any two cavities are aligned with their two corresponding bumps when a temperature of the reflow process reaches a melting point of the bumps.

[c11] 11. The flip-chip bonding process of claim 10, wherein the substrate has a coefficient of thermal expansion greater than that of the chip.

[c12] 12. The flip-chip bonding process of claim 11, wherein a distance between any two bumps is greater than a distance between their two corresponding cavities at room temperature.

[c13] 13. The flip-chip bonding process of claim 10, wherein the first expansion reference mark is located at a center of a distribution region of the cavities.

[c14] 14. The flip-chip bonding process of claim 10, wherein

the second expansion reference mark is located at a center of a distribution region of the bumps.

[c15] 15. A chip for bonding with a substrate, wherein the substrate has a plurality of contact pads and a plurality of cavities, each contact pad being exposed by one cavity, the chip comprising:
a plurality of bonding pads on an active surface of the chip with a bump on each bonding pad, wherein any two of the bumps are aligned to the corresponding two cavities on the substrate.

[c16] 16. The chip of claim 15, wherein the substrate has a coefficient of thermal expansion greater than that of the chip.

[c17] 17. The chip of claim 16, wherein a distance between any two bumps is greater than a distance between their two corresponding cavities at room temperature.

[c18] 18. The chip of claim 15, wherein the cavities are arranged in arrays.

[c19] 19. The chip of claim 15, wherein the bumps are arranged in arrays.

[c20] 20. The chip of claim 15, wherein one of the contact pads serves as a first expansion reference mark and one

of the bonding pads corresponding to the first expansion reference mark serves as a second expansion reference mark such that the first expansion reference mark on the substrate is aligned to the second expansion reference mark on the chip.

[c21] 21. The chip of claim 20, wherein the first expansion reference mark is located at a center of a distribution region of the cavities.

[c22] 22. The chip of claim 20, wherein the second expansion reference mark is located at a center of a distribution region of the bumps.